Notice of Allowability	Application No.	Applicant(s)	
	09/388,766	SHIH ET AL.	
	Examiner	Art Unit	
	Ayal I. Sharon	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment filed 6/27/05*.

2. ☒ The allowed claim(s) is/are *1-25 and 29-35*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Introduction

1. Claims 1-35 of U.S. Application 09/388,766, originally filed on 09/02/1999 are presented for examination. The Amendment filed 11/24/2004 contains amendments to claims 15, 20, 24, 25, 33, and 34. Claims 26-28 were cancelled. Claim 29 was corrected. (see p.11 of amendment for discussion of this correction). No new claims were added.
2. Applicant's arguments presented in the amendment filed 6/27/05 have been found to be persuasive. The claims have been allowed.

Claim Interpretations

3. Examiner has interpreted the claims according to the definitions specified in detail in the "Claim Interpretations" section of the previous Office Action.

Examiner's Statement of Reasons for Allowance

4. Claims 1-25, and 29-35 are allowed.
5. The following is the examiner's statement of reasons for allowance.
6. The prior art referred to in this Reasons for Allowance is as follows:

- U.S. Patent 6,542,860 to McBride. (Filed March 22, 1999). Hereinafter "**McBride**". McBride teaches a system and method for detecting nodes that are susceptible to floating.
- U.S. Patent 6,090,149 to Nair et al. (Filed Feb. 19, 1998). Hereinafter "**Nair**". Nair teaches a system and method for detecting floating nodes within a simulated integrated circuit.

7. In regards to the following limitations of Claim 1,

> *1. (Previously Presented) A method of simulating a node using a simulation program that includes multiple, linked modules, the method comprising:*
>
> *executing a first circuit module that simulates a circuit having a node, wherein the node represents a simulated electrical connection point of the circuit;*
>
> *simultaneously executing at least one behavior module, which is linked to the first circuit module, and which performs the acts of*

Both McBride and Nair teach the identification of "nodes susceptible to floating in a manner that may be adverse to surrounding circuit components" (McBride, col.9, lines 38-43 and 59-62; col.10, lines 13-21 and 27-30) and "detecting floating transistor gates within a netlist" (Nair, col.2, lines 16-18).

The two references differ in that McBride uses data structures to determine if any of the gates are "pass FETs" (See col.9, line 50 to col.10, line 20). If such a structure is identified, McBride then lists it in an error report to alert of potential design problems (col.10, lines 27-30).

Nair, on the other hand, runs a circuit simulation twice: once with and a "resistor card" attached, and once without (col.6, lines 1-20). In both cases,

currents are measured. It is the attaching of the resistor card that "forces" the voltages in the circuits (col.6, lines 33-36).

A third set of currents is determined using a formula (col.6, lines 1-20). Once the three currents are known, comparisons can be made. In order to determine which nodes in the circuit may be floating, the output file of the simulation using the resistor card is searched for nodes having a voltage value close to (VCC-VSS)/2 (See col.6, lines 41-47; and Fig.6, Item 66).

Therefore, Nair teaches the following limitations, while McBride does not:

> *forcing an initial forced logic state on the node;*
>
> *after forcing, releasing the node from the initial forced logic state if a predetermined condition is met, which enables the simulation program to change a logic state of the node;*

However, neither McBride nor Nair teach the following sequence of limitations:

> *monitoring the node after the node has been released; and*
>
> *providing an indication, in response to the monitoring, when the node is in a preselected condition.*

McBride does not expressly teach testing for "valid logic values." It scans the netlist looking for "pass FETs" (See col.9, line 50 to col.10, line 20).

Nair runs two separate simulations and compares results. The instant application, on the other hand, runs one continuous simulation, and monitors the results of releasing the forced signal. (See Fig.8, Item 420 and page 10 of the specification, lines 13-21). The Nair reference does not teach the continuous monitoring of the node that is described and claimed in the instant invention.

8. Dependent Claims 2-7 depend from allowable claim 1, and are therefore allowable.

9. In regards to the following limitations of Claim 8,

> *8.(Previously Presented) A method of initializing and monitoring a simulated circuit node using a simulation program that includes multiple, linked modules, the method comprising:*
>
> *executing a first circuit module that simulates a circuit having a node, wherein the node represents a simulated electrical connection point of the circuit;*
>
> *simultaneously executing at least one behavior module, which is linked to the first circuit module, and which performs the acts of*
>
> *obtaining an initial node condition for the node, wherein the initial node condition is a logic state;*
>
> *forcing the node to the initial node condition;*
>
> *after forcing, releasing the node from the initial node condition;*
>
> *testing the node for a valid condition after the node has been released;*
>
> *monitoring the node after the node has been released; and*
>
> *providing an indication, in response to the monitoring,, when the node is in an undesirable condition.*

Neither McBride nor Nair teach the monitoring of the node. This is described in detail in the reasons for allowance of Claim 1.

10. Dependent Claims 9-14 depend from allowable claim 8, and are therefore allowable.

11. In regards to the following limitations of Claim 15,

> *15. (Currently Amended) A computer-readable medium having computer-executable instructions comprising:*
>
> *at least one selectable circuit module, which when executed simulates a circuit having a node, wherein the node represents a simulated electrical connection point of the circuit; and*

at least one selectable behavior module, which is linkable to a circuit module, and which when executed simultaneously with the at least one selectable circuit module results in performing the following acts:

forcing an initial forced logic state on the node;

after forcing, releasing the node from the initial forced logic state if a predetermined condition is met, which enables a simulation program to change a logic state of the node;

monitoring the node after the node has been released; and providing an indication, in response to the monitoring,

when the node is in a preselected condition.

Neither McBride nor Nair teach the monitoring of the node. This is described in detail in the reasons for allowance of Claim 1.

12. Dependent Claims 16-19 depend from allowable claim 15, and are therefore allowable.

13. In regards to the following limitations of Claim 20,

20. (Currently Amended) A simulation module of a simulation program, the simulation module comprising:

an input means for inputting an initial node condition into a simulated circuit node of a circuit module linked with and simultaneously executable with the simulation module, wherein the simulated circuit node represents a simulated electrical connection point of the circuit module;

a conveying means for conveying the initial node condition to the simulated circuit node;

release means for releasing the simulated circuit node from the initial node condition upon satisfaction of a condition, wherein releasing the simulated circuit node occurs after conveying and enables the simulation program to change a logic state of the simulated circuit node;

a monitoring means for monitoring the simulated circuit node for a node condition after releasing the simulated circuit node from the initial node condition; and

an output means, responsive to the monitoring means, for outputting an indication when the node condition is in an undesirable state.

Neither McBride nor Nair teach the monitoring of the node. This is described in detail in the reasons for allowance of Claim 1.

14. Dependent Claims 21-23 depend from allowable claim 20, and are therefore allowable.

15. In regards to the following limitations of Claim 24,

> *24.(Currently Amended) A computerized system for initializing and monitoring a simulated circuit node, the system comprising:*
>
> *a circuit simulation tool;*
>
> *at least one selectable circuit module, which when executed simulates a circuit having the simulated circuit node, wherein the simulated circuit node represents a simulated electrical connection point of the circuit; and*
>
> *at least one selectable behavior module, which is linkable to and simultaneously executable with a circuit module, and which includes a first input means for inputting an initial node condition;*
>
> *a conveying means for conveying the initial node condition to the simulated circuit node;*
>
> *a release means for releasing the initial node condition, wherein releasing the initial node condition occurs after conveying and enables the circuit simulation tool to change a logic state of the simulated circuit node;*
>
> *a monitoring means for monitoring the simulated circuit node for a node condition after releasing the initial node condition; a first output means for outputting an indication when the node condition is in an undesirable state, in response to the monitoring;*
>
> *a second input means for inputting a simulation run time; and*
>
> *a second output means for outputting a final node condition at completion of the simulation run time.*

Neither McBride nor Nair teach the monitoring of the node. This is described in detail in the reasons for allowance of Claim 1.

16. In regards to the following limitations of Claim 25,

> *25. (Currently Amended) An HDL initial condition module comprising: a means for maintaining a logic level of a simulated circuit node until a release condition is met, wherein*
>
> *the simulated circuit node represents a simulated electrical connection point of a simulated circuit, and the simulated circuit is produced by an HDL circuit module that is linkable to the HDL initial condition module, and*
>
> *a simulation program is able to change a logic state of the simulated circuit node after the release condition is met, wherein the release condition is when a known logic state can be determined for the simulated circuit node;*
>
> *an initial condition release means, which enables the simulation program to change the logic level after the release condition is met; and*
>
> *a simulated circuit node error detection means, which monitors the simulated circuit node for a node condition.*

Both McBride and Nair teach the identification of "nodes susceptible to floating in a manner that may be adverse to surrounding circuit components" (McBride, col.9, lines 38-43) and "detecting floating transistor gates within a netlist" (Nair, col.2, lines 16-18).

However, neither McBride nor Nair expressly teach the following limitations:

> *the simulated circuit node represents a simulated electrical connection point of a simulated circuit, and the simulated circuit is produced by an HDL circuit module that is linkable to the HDL initial condition module, and*

Neither McBride nor Nair expressly teach that their inventions are expressly implemented in the specific arrangement of HDL modules and sub-modules that are recited in Claim 25.

McBride makes a passing mention to the use of HDL in designing circuits (see col.2, lines 5-15), but implements his invention in the commercially available

software PathMill (see col.2, lines 29-41), and not in a system of HDL modules recited in Claim 25.

Nair expressly teaches the use of net lists and products such as SPICE and STAR-SIM™ (see col.1, lines 58-67), but is silent as to the use of HDL for modeling circuits, and does not teach a system of HDL modules as recited in Claim 25.

Moreover, neither McBride nor Nair teach the monitoring of the node. This is described in detail in the reasons for allowance of Claim 1.

17. Dependent Claims 29-30 depend from allowable claim 25, and are therefore allowable.

18. In regards to the following limitations of Claim 31,

31. (Previously Presented) An HDL simulated circuit device, comprising: a circuit HDL module, which when executed simulates a circuit having a first simulated node, wherein the first simulated node represents a simulated electrical connection point of the circuit;

a first HDL module, linked to the circuit HDL module, the first HDL module including
a first input submodule inputting a first initial node condition,
a first conveyance submodule conveying the first initial node condition to the first simulated node,
a first monitor submodule monitoring the first simulated node for a first node condition, wherein monitoring occurs after conveying, and
a first output submodule outputting, in response to monitoring,
a first indication when the first node condition is in an undesirable state;

a second HDL module, linked to the circuit HDL module, the second HDL module including
a second input submodule inputting a second initial node condition,
a second conveyance submodule conveying the second initial node condition to a second simulated node,
a release submodule releasing the second simulated node on a predetermined condition, wherein releasing the second simulated node enables a simulation program to change a logic level of the second simulated node,
a second monitor submodule monitoring the second simulated node for a second node condition, wherein monitoring occurs after releasing, and

a second output submodule outputting, in response to monitoring, a second indication when the second node condition is in an undesirable state; and wherein the first conveyance submodule additionally conveys the first initial node condition to the second input submodule.

Neither McBride nor Nair expressly teach that their inventions are expressly implemented in the specific arrangement of HDL modules and sub-modules that are recited in Claim 31.

Moreover, neither McBride nor Nair teach the monitoring of the node. This is described in detail in the reasons for allowance of Claim 1.

19. In regards to the following limitations of Claim 32,

32. (Previously Presented) An HDL simulated circuit device, comprising:

a circuit HDL module, which when executed, simulates a circuit having a first simulated node, wherein the first simulated node represents a simulated electrical connection point of the circuit;

a first HDL module, linked to the circuit HDL module, the first HDL module including

a first input means for inputting a first initial node condition,

a first conveyance means for conveying the first initial node condition to the first simulated node, and

a first node condition output means for outputting a first indication when a first node condition is in an undesirable state, wherein outputting occurs after conveying;

a second HDL module, linked to the circuit HDL module, the second HDL module including

a second input means for inputting a second initial node condition and

a second conveyance means for conveying the second initial node condition to a second simulated node; and

a third HDL module, linked to the circuit HDL module, the third HDL module including

a release condition means for releasing the second simulated node on a release condition, wherein releasing the second simulated node occurs after conveying and enables a simulation program to change a logic level of the second simulated node,

wherein the first node condition output means outputs the first node condition to the second input means if the release condition is valid.

Neither McBride nor Nair expressly teach that their inventions are expressly implemented in the specific arrangement of HDL modules and sub-modules that are recited in Claim 32. (The limitations that are taught by McBride and Nair are described in detail in the reasons for allowance of Claim 31).

Moreover, neither McBride nor Nair teach the monitoring of the node. This is described in detail in the reasons for allowance of Claim 1.

20. In regards to the following limitations of Claim 33,

33. (Currently Amended) An HDL design tool, comprising:

a circuit simulation device; and

a plurality of selectable modules capable of being linked to the circuit simulation device, wherein the plurality of selectable modules includes at least one selectable behavior module, which is linkable to a circuit module, and which when executed simultaneously results in

inputting an initial node condition into a simulated circuit node of the circuit module linked with the behavior module, wherein the simulated circuit node represents a simulated electrical connection point of the circuit module,

conveying the initial node condition to the simulated circuit node,

releasing the simulated circuit node from the initial node condition if a condition is met, wherein releasing the simulated circuit node occurs after conveying and enables the circuit simulation device to change a logic state of the simulated circuit node,

monitoring the simulated circuit node for a node condition, wherein monitoring occurs after releasing, and

outputting an indication, in response to monitoring, when the node condition is in an undesirable state.

Neither McBride nor Nair expressly teach that their inventions are expressly implemented in the specific arrangement of HDL modules and sub-

modules that are recited in Claim 32. (The limitations that are taught by McBride and Nair are described in detail in the reasons for allowance of Claim 31).

Moreover, neither McBride nor Nair teach the monitoring of the node. This is described in detail in the reasons for allowance of Claim 1.

21. In regards to the following limitations of Claim 34,

> *34. (Currently Amended) A simulation method, comprising:*
>
> *executing phase one by a behavior module, including*
>
> *forcing an initial logic zero, logic one or high-impedance on a node of a circuit module linked with the behavior module, wherein the node represents a simulated electrical connection point of the circuit module,*
>
> *releasing the node, wherein releasing the node enables a simulation program to change a logic state of the node, and wherein releasing occurs after forcing,*
>
> *testing to see if the node has a valid logic value, wherein testing occurs after releasing,*
>
> *if the node has the valid logic value, continuing to phase two, and*
>
> *if the node does not have the valid logic value, continuing in phase one; and simultaneously executing phase two by the behavior module, including*
>
> *monitoring the node value,*
>
> *testing the node value for a valid condition,*
>
> *indicating an error if an unacceptable condition appears on the node, in response to monitoring and testing, and*
>
> *continuing in phase two until simulation completion.*

Neither McBride nor Nair teach the monitoring of the node. This is described in detail in the reasons for allowance of Claim 1.

22. Dependent Claim 35 depends from allowable independent claim 34.

23. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should

preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (571) 272-3714. The examiner can normally be reached on Monday through Thursday, and the first Friday of a bi-week, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached at (571) 272-3749.

Any response to this office action should be faxed to (571) 273- 8300, or mailed to:

USPTO
P.O. Box 1450
Alexandria, VA 22313-1450

or hand carried to:

USPTO Customer Service Window
Randolph Building
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Alexandria, VA 22314

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center 2100 Receptionist, whose telephone number is (571) 272-2100.

Ayal I. Sharon
Art Unit 2123
September 21, 2005

Paul L. Rodriguez 9/21/05
Primary Examiner
Art Unit 2125